REMARKS

In response to the Office Action mailed December 11, 2006, Applicant respectfully requests reconsideration. Claims 1-8 were previously pending in this application. By this amendment, claims 1 and 4-8 have been amended. New claims 9-12 have been added. As a result, claims 1-12 are pending for examination with claims 1, 5, 7 and 8 being independent. No new matter has been added.

Telephone Interview with Examiner Romano

Applicant's representatives thank Examiner Romano for the courtesies extended in granting and conducting a telephone interview held on April 26, 2007. During the interview, Applicant's representatives discussed with the Examiner claims as currently pending and the cited references. The substance of the telephone interview is summarized below in response to the rejections raised in the Office Action.

Rejections Under 35 U.S.C. §103

The Office Action rejected claims 1-8 under 35 U.S.C. §103(a) as being unpatentable over Hadjiyiannis et al., "ISDL: An Instruction Set Description Language for Retargetability," (hereinafter Hadjiyiannis) and further in view of Vos, GB 2,127,188A (hereinafter Vos). Applicant respectfully traverses the rejection.

During the telephone interview, the Examiner suggested that independent claims 1, 5, 7 and 8 be amended to recite in more detail a process of constraining the machine language to conform to an architecture of the instruction set. Accordingly, claims 1 and 4-8 have been amended to more clearly distinguish over the cited references. Support for these amendments can be found, for example, on page 10, lines 18-30 and in Figs. 4-6 of the present application. In addition, new claims 9-12 have been added, with claims 9 and 10 being dependent from claim 7 and claims 11 and 12 being dependent from claim 1.

Claim 1, as amended, recites:

> An assembler for a target microprocessor, the assembler comprising:

a descriptor of the assembler file containing information descriptive of an instruction set of said target microprocessor, *wherein at least one instruction in the instruction set is aligned with a starting position of a bit field*;

a translation device of the assembler for translating assembly language instructions into machine language as an output;

a fetching device of the assembler for acquiring data from said descriptor file;

a control device of the assembler arranged to receive said data from said fetching device and said machine language from said translation device, and operable to constrain the machine language to conform to an architecture of said instruction set, *wherein the machine language is constrained using the at least one instruction in the instruction set that is aligned with the starting position of the bit field*; and

a data transfer device of the assembler arranged to output selected data fetched from said descriptor file directly to a linker.

(Emphasis added).

Hadjiyiannis is directed to a language called ISDL (Instruction Set Description Language) that can be used to describe target architectures in a re-targetable compiler. The ISDL description of a target architecture can be used to generate an assembler (Section III, paragraph 1, lines 7-8). Hadjiyiannis discusses an automatic assembler generator that receives an ISDL description as input, and produces an assembler which assembles the compiler's output to a binary file (Section V, paragraph 2, lines 1-3).

Vos is directed to a system for translating hardware/software interface specifications simultaneously into specific microprocessor executable code and commands for the linker/loading system of a selected hardware configuration (page 1, lines 5-9).

Neither Hadjiyiannis nor Vos discloses or suggests "an assembler for a target microprocessor, the assembler comprising: a descriptor of the assembler file containing information descriptive of an instruction set of said target microprocessor, wherein at least one instruction in the instruction set is aligned with a starting position of a bit field; a translation device of the assembler for translating assembly language instructions into machine language as an output; a fetching device of the assembler for acquiring data from said descriptor file; a control device of the assembler arranged to receive said data from said fetching device and said machine language from said translation device, and operable to constrain the machine language to conform to an architecture of said instruction set, wherein the machine language is constrained using the at least one instruction in the instruction set that is aligned with the starting position of the bit field; and a data transfer device

of the assembler arranged to output selected data fetched from said descriptor file directly to a linker," as recited in claim 1.

In view of the foregoing, claim 1 patentably distinguishes over Hadjiyiannis and Vos, either alone or in combination.

Claims 2-4 depend from claim 1 and are allowable for at least the same reasons.

Accordingly, withdrawal of the rejection of claims 1-4 is respectfully requested.

Claim 5, as amended, recites:

> A method of assembling a machine language program for a target microprocessor comprising:
> providing a descriptor file containing information descriptive of an instruction set of said target microprocessor, *wherein at least one instruction in the instruction set is aligned with a starting position of a bit field*;
> translating assembly language instructions into machine language wherein the translation comprises:
> directly transliterating the assembly language instructions to machine language;
> acquiring data from said descriptor file;
> constraining the directly transliterated machine language to conform to an architecture of said instruction set, thereby assembling the machine language program for the target microprocessor, *wherein the machine language is constrained using the at least one instruction in the instruction set that is aligned with the starting position of the bit field*; and
> transferring selected data acquired from said descriptor file directly to a linker.
> (Emphasis added).

Neither Hadjiyiannis nor Vos discloses or suggests "a method of assembling a machine language program for a target microprocessor comprising: providing a descriptor file containing information descriptive of an instruction set of said target microprocessor, wherein at least one instruction in the instruction set is aligned with a starting position of a bit field; translating assembly language instructions into machine language wherein the translation comprises: directly transliterating the assembly language instructions to machine language; acquiring data from said descriptor file; constraining the directly transliterated machine language to conform to an architecture of said instruction set, thereby assembling the machine language program for the target microprocessor, wherein the machine language is constrained using the at least one instruction in

the instruction set that is aligned with the starting position of the bit field; and transferring selected data acquired from said descriptor file directly to a linker," as recited in claim 5.

In view of the foregoing, claim 5 patentably distinguishes over Hadjiyiannis and Vos, either alone or in combination.

Claim 6 depends from claim 5 and is allowable for at least the same reasons.

Accordingly, withdrawal of the rejection of claims 5 and 6 is respectfully requested.

Claim 7, as amended, recites:

> A method of preparing a program executable on a target microprocessor comprising:
>
> capturing data from an instruction set of said target microprocessor thereby forming a descriptor file containing information descriptive of said instruction set, *wherein at least one instruction in the instruction set is aligned with a starting position of a bit field*;
>
> providing assembly language instructions for said target microprocessor;
>
> translating each assembly language instruction into a corresponding machine language output;
>
> using data from said descriptor file, constraining the machine language output to conform to an architecture of said instruction set, *wherein the machine language is constrained using the at least one instruction in the instruction set that is aligned with the starting position of the bit field*; and
>
> transferring selected data from said descriptor file directly to a linker.
>
> (Emphasis added).

Neither Hadjiyiannis nor Vos discloses or suggests "a method of preparing a program executable on a target microprocessor comprising: capturing data from an instruction set of said target microprocessor thereby forming a descriptor file containing information descriptive of said instruction set, wherein at least one instruction in the instruction set is aligned with a starting position of a bit field; providing assembly language instructions for said target microprocessor; translating each assembly language instruction into a corresponding machine language output; using data from said descriptor file, constraining the machine language output to conform to an architecture of said instruction set, wherein the machine language is constrained using the at least one instruction in the instruction set that is aligned with the starting position of the bit field; and transferring selected data from said descriptor file directly to a linker," as recited in claim 7.

In view of the foregoing, claim 7 patentably distinguishes over Hadjiyiannis and Vos, either alone or in combination.

Accordingly, withdrawal of the rejection of claim 7 is respectfully requested.

Claim 8, as amended, recites:

> A method of preparing a program executable on a microprocessor, comprising:
> providing plural program modules, at least one of said modules having one or more instructions including external symbols, wherein external symbols have values which cannot be determined without reference to another program module;
> providing a descriptor file containing information descriptive of an instruction set of said target microprocessor, *wherein at least one instruction in the instruction set is aligned with a starting position of a bit field*;
> translating assembly language instructions into machine language wherein the translation comprises:
> directly transliterating the assembly language instructions into machine language;
> acquiring data from said descriptor file; and
> constraining the directly transliterated machine language to conform to an architecture of said instruction set, *wherein the directly transliterated machine language is constrained using the at least one instruction in the instruction set that is aligned with the starting position of the bit field*;
> transferring selected data acquired from said descriptor file directly to a linker; and
> binding external symbols to addresses using data selected from said descriptor file, thereby preparing the program executable on the microprocessor.
> (Emphasis added).

Neither Hadjiyiannis nor Vos discloses or suggests "a method of preparing a program executable on a microprocessor, comprising: providing plural program modules, at least one of said modules having one or more instructions including external symbols, wherein external symbols have values which cannot be determined without reference to another program module; providing a descriptor file containing information descriptive of an instruction set of said target microprocessor, wherein at least one instruction in the instruction set is aligned with a starting position of a bit field; translating assembly language instructions into machine language wherein the translation comprises: directly transliterating the assembly language instructions into machine language; acquiring data from said descriptor file; and constraining the directly transliterated machine language to conform to an architecture of said instruction set, wherein the directly transliterated machine language is constrained using the at least one instruction in the instruction set that is aligned with the starting position of the bit field; transferring selected data acquired from said

descriptor file directly to a linker; and binding external symbols to addresses using data selected from said descriptor file, thereby preparing the program executable on the microprocessor," as recited in claim 8.

In view of the foregoing, claim 8 patentably distinguishes over Hadjiyiannis and Vos, either alone or in combination.

Accordingly, withdrawal of the rejection of claim 8 is respectfully requested.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

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Respectfully submitted,

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